WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected;

a resin molding said portion to be connected; and

a member electrically connected to said connected member in which an alloy layer having a melting point higher than that of a solder having Pb as a main composition metal and containing no Pb as a main composing metal is provided at a portion outside said resin.

2. A semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and an alloy layer having a melting point higher than that of a solder having Pb as a main composition metal and containing no Pb as a main composing metal is provided at a portion outside a portion molded by a resin; and

a resin molding said connected portion.

3. A semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and a metal layer having a melting point higher than that of an Sn-Pb eutectic solder and containing no Pb and Pd as a main composing metal is provided at a portion outside a portion molded by a resin; and

a resin molding said connected portion.

4. A semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and a Pb-free metal layer having a melting point higher than that of an Sn-Pb eutectic solder and containing no Pd as a main composing metal is provided at a portion outside a portion molded by a resin; and

a resin molding said connected portion.

5. A semiconductor integrated circuit device comprising:

a semiconductor chip;

a connecting member connected to said semiconductor chip and having a conductivity;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and a Pb-

free metal layer having a melting point higher than that of an Sn-Pb eutectic solder and containing no Pd as a main composing metal is provided in the other portions;

a resin molding a portion of said semiconductor chip connected to said connecting portion, said connecting member and a portion of said connected portion to which said connecting member is connected.

6. A semiconductor integrated circuit device comprising:

a semiconductor chip;

a wire bonded to said semiconductor chip;

a lead in which a metal layer including a palladium layer is plated on a portion in an inner lead bonded by said wire, a Pb-free alternate solder having a melting point higher than that of an Sn-Pb eutectic solder and containing no Pd as a main composing metal is plated on a mounted portion of an outer lead;

a resin molding a bonding portion of said semiconductor chip to which said wire is bonded, said wire and the inner lead of said lead including a portion to which said wire is bonded.

7. A semiconductor integrated circuit device comprising:

a semiconductor chip;

a wire;

a resin molding said semiconductor chip and

said wire; and

a lead in which a metal layer including a palladium layer is provided in a front end of a portion molded by said resin, and a Pb-free metal layer having a melting point higher than an Sn-Pb eutectic solder and containing no Pd as a main composing metal is provided in a portion outside a portion molded by said resin.

8. A semiconductor integrated circuit device comprising:

a semiconductor chip;

a lead in which a front end portion of an inner lead is plated by Pd and an outer lead is plated by a Pb-free solder;

a wire bonding said semiconductor chip and the inner lead of said lead; and

a resin molding said semiconductor chip, the inner lead portion of said lead and said wire,

wherein a melting point of said Pb-free alternate solder is higher than a melting point of an Sn-Pb eutectic solder, and said Pb-free alternate solder is not composed of only Pd.

9. A mounting substrate comprising:

a semiconductor integrated circuit device, said semiconductor integrated circuit device being provided with a connecting member having a conductivity, a connected member in which a metal layer including a palladium layer is provided at a portion to

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which said connecting member is connected, and an alloy containing no Pb as a main composing metal is provided outside a portion molded by a resin, and a resin molding said portion to be connected; and

a printed circuit board,

wherein said semiconductor integrated circuit device is connected to said printed circuit board by a solder having a melting point higher than that of the solder having Pb as a main composing metal.

10. A mounting substrate comprising:

a semiconductor integrated circuit device, said semiconductor integrated circuit device being provided with a connecting member having a conductivity, a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and a metal containing no Pb as a main composing metal is provided outside a portion molded by a resin, and a resin molding said portion to be connected; and

a printed circuit board to which said semiconductor integrated circuit device is connected by a metal having a melting point higher than that of the solder having Pb as a main composing metal.

11. A method of manufacturing a mounting substrate, said mounting substrate comprising:

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a semiconductor integrated circuit device, said semiconductor integrated circuit device being provided with a connecting member having a

conductivity, a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and an alloy layer containing no Pb as a main composing metal is provided outside a portion molded by a resin, and a resin molding said portion to be connected; and

a printed circuit board,

wherein said method has a process at which a temperature of said connected member becomes higher than a melting point of an Sn-Pb eutectic solder.

12. A method of manufacturing a mounting substrate, said mounting substrate comprising:

a semiconductor integrated circuit device,

said semiconductor integrated circuit device being provided with a connecting member having a conductivity, a connected member in which a metal layer including a palladium layer is provided at a portion to which said connecting member is connected, and an alloy layer containing no Pb as a main composing metal is provided outside a portion molded by a resin, and a resin molding said portion to be connected; and

a printed circuit board,

wherein said semiconductor integrated circuit device and said printed circuit board are received within the same furnace and a temperature within said furnace becomes higher than a melting point of an Sn-Pb eutectic solder.

13. A method of manufacturing a mounting

substrate, said mounting substrate comprising:

a semiconductor integrated circuit device provided with a semiconductor chip, a lead in which a Pd metal is plated on a front end portion of an inner lead and a Pb-free metal is plated on an outer lead, a wire bonding said semiconductor chip and said lead, and a resin molding a wire bonding portion of said semiconductor chip, a wire bonding portion of said lead and said wire, wherein a melting point of said Pb-free alternate solder is higher than a melting point of an Sn-Pb eutectic solder, and said Pb-free alternate solder is not composed of only Pd; and

a printed circuit board,

wherein said semiconductor integrated circuit device and said printed circuit board are received in a reflow furnace, and a set temperature of the reflow furnace is higher than a set temperature at a time of reflow mounting the semiconductor integrated circuit device in which a Pb metal layer is provided in an outer lead, to the substrate.

14. A semiconductor integrated circuit device comprising:

a wire having a diameter equal to or less than 30 μm;

a connected member in which a metal layer including a palladium layer is provided at a portion to which said wire is connected, and a solder containing Pb as a main composition metal is provided at a portion

outside a portion molded by a resin; and

a resin for molding said connected portion.

15. A mounting substrate comprising:

a semiconductor integrated circuit device provided with a semiconductor chip, a lead in which a Pd metal is attached and formed onto a front end portion of an inner lead and a Pb solder layer is attached and formed onto an outer lead, a wire bonding said semiconductor chip and said lead and having a diameter of 30 μm or less, and a resin molding a wire bonding portion of said semiconductor chip, a wire bonding portion of said lead and said wire; and

a printed circuit board.

16. A semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a connected member in which a metal layer is provided in a portion to which said connecting member is adhered; and

a resin molding said adhered portion,

wherein a thickness of the adhered portion in said connecting member is equal to or more than 10 μm.

17. A method of manufacturing a plurality of semiconductor integrated circuit devices, said semiconductor integrated circuit device comprising:

a connecting member having a conductivity;

a resin; and

a connected member in which a first metal

layer is provided in a portion to which said connecting member is connected, and a second metal layer different from said first metal layer is provided outside a portion molded by said resin, and a resin molding said portion to be connected,

wherein there is provided a process of attaching and forming a metal layer having a difference between a thickness of the first metal layer of a first semiconductor integrated circuit device and a thickness of the first metal layer of a second semiconductor integrated circuit device is less than 10 μm.

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